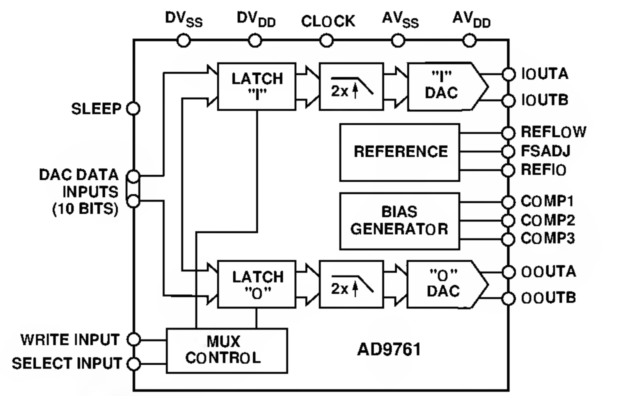
# Dual 10-Bit TxDAC™ * with 2× Interpolation Filters

# AD9761

**FEATURES**
- **Complete 10-Bit, 40 MSPS Dual Transmit DAC**
- **Excellent Gain and Offset Matching**
- **Differential Nonlinearity Error: 0.5 LSB**
- **Signal-to-Noise and Distortion Ratio: 58 dB**
- **Spurious-Free Dynamic Range: –65 dB**
- **2× Interpolation Filters**
- **20 MSPS/Channel Data Rate**
- **Single Supply: +2.7 V to +5.5 V**
- **Low Power Dissipation: 200 mW (+3 V Supply @ 40 MSPS)**
- **On-Chip Reference**
- **28-Lead SSOP**

**FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD9761 is a complete dual channel, high speed, 10-bit CMOS DAC. The AD9761 has been developed specifically for use in wide bandwidth communication applications (e.g., spread spectrum) where digital I and Q information is being processed during transmit operations. It integrates two 10-bit, 40 MSPS DACs, dual 2× interpolation filters, a voltage reference, and digital input interface circuitry. The AD9761 supports a 20 MSPS per channel input data rate which is then interpolated up to 40 MSPS before simultaneously updating each DAC.

The interleaved I and Q input data stream is presented to the digital interface circuitry which consists of I and Q latches as well as some additional control logic. The data is de-interleaved back into its original I and Q data. An on-chip state machine ensures the proper pairing of I and Q data. The data output from each latch is then processed by a 2× digital interpolation filter which eases the reconstruction filter requirements. The interpolated output of each filter serves as the input of their respective 10-bit DAC.

The DACs utilize a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and to maximize dynamic accuracy. Each DAC provides differential current output thus supporting single-ended or differential applications. Both DACs are simultaneously updated and provide a nominal full-scale current of 10 mA. Also, the full-scale currents between each DAC are matched to within 0.02 dB (i.e., 0.19%), thus eliminating the need for additional gain calibration circuitry.

The AD9761 is manufactured on an advanced low cost CMOS process. It operates from a single supply of 2.7 V to 5.5 V and consumes 250 mW of power. To make the AD9761 complete it also offers an internal 1.20 V temperature compensated bandgap reference.

## PRODUCT HIGHLIGHTS

1. Dual 10-bit, 40 MSPS DACs: A pair of high performance 40 MSPS DACs optimized for low distortion performance provide for flexible transmission of I and Q information.
2. 2× Digital Interpolation Filters: Dual matching FIR interpolation filters with 62.5 dB stop band rejection precede each DAC input thus reducing the DACs' reconstruction filter requirements.
3. Low Power: Complete CMOS Dual DAC function operates off of a low 200 mW on a single supply from 2.7 V to 5.5 V The DAC full scale current can be reduced for lower power operation, and a sleep mode is provided for power reduction during idle periods.
4. On-Chip Voltage Reference: The AD9761 includes a 1.20 V temperature compensated bandgap voltage reference.
5. Single 10-Bit Digital Input Bus: The AD9761 features a flexible digital interface allowing each DAC to be addressed in a variety of ways including different update rates.
6. Small Package: The AD9761 offers the complete integrated function in a compact 28-lead SSOP package.
7. Product Family: The AD9761 Dual Transmit DAC has a pair of Dual Receive ADC companion products, the AD9281 (8 bits) and AD9201 (10 bits).

REV. 0



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# AD9761–SPECIFICATIONS

## DC SPECIFICATIONS ($T_{MIN}$ to $T_{MAX}$, AVDD = +5 V, DVDD = +5 V, $I_{OUTFS}$ = 10 mA, unless otherwise noted)

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| RESOLUTION | 10 | | | Bits |
| DC ACCURACY[1] | | | | |
| Integral Linearity Error (INL) | | | | |
| $T_A$ = +25°C | | 1 | | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | | |
| DIFFERENTIAL (DNL) | | | | |
| $T_A$ = +25°C | | 0.5 | | LSB |
| $T_{MIN}$ to $T_{MAX}$ | | | | |
| Monotonicity (10-Bit) | GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE | | | |
| ANALOG OUTPUT | | | | |
| Offset Error | | ±0.025 | | % of FSR |
| Offset Matching between DACs | | | | % of FSR |
| Gain Error (Without Internal Reference) | | | | % of FSR |
| Gain Error (With Internal Reference) | | | | % of FSR |
| Gain Matching between DACs | | | | % of FSR |
| Full-Scale Output Current[2] | | 10 | | mA |
| Output Compliance Range | | 1.25 | | V |
| Output Resistance | | 100 | | kΩ |
| Output Capacitance | | 5 | | pF |
| REFERENCE OUTPUT | | | | |
| Reference Voltage | | 1.20 | | V |
| Reference Output Current[3] | | 1 | | μA |
| REFERENCE INPUT | | | | |
| Input Compliance Range | 0.1 | | 1.25 | V |
| Reference Input Resistance | | 1 | | MΩ |
| TEMPERATURE COEFFICIENTS | | | | |
| Unipolar Offset Drift | | 0 | | ppm/°C |
| Gain Drift (without Internal Reference) | | ±50 | | ppm/°C |
| Gain Drift (with Internal Reference) | | ± 100 | | ppm/°C |
| Gain Matching Drift (Between DACs) | | | | ppm/°C |
| Reference Voltage Drift | –100 | | 100 | ppm/°C |
| POWER SUPPLY | | | | |
| AVDD | | | | |
| Voltage Range | 2.7 | 5.0 | 5.5 | V |
| Analog Supply Current ($I_{AVDD}$) | | 25 | 35 | mA |
| DVDD | 2.7 | 5.0 | 5.5 | V |
| Voltage Range | 2.7 | 5.0 | 5.5 | V |
| Digital Supply Current at 5 V ($I_{DVDD}$)[4] | | 70 | 80 | mA |
| Digital Supply Current at 3 V ($I_{DVDD}$)[4] | | 35 | 40 | mA |
| Nominal Power Dissipation[5] | | | | |
| AVDD and DVDD at 3 V | | 200 | 230 | mW |
| AVDD and DVDD at 5 V | | 500 | 650 | mW |
| Power Supply Rejection Ratio (PSRR)–AVDD | –0.2 | | +0.2 | % of FSR/V |
| Power Supply Rejection Ratio (PSRR)–DVDD | –0.025 | | +0.025 | % of FSR/V |
| OPERATING RANGE | –40 | | +85 | °C |



NOTES
[1]Measured at IOUTA and QOUTA, driving a virtual ground.
[2]Nominal full-scale current, IOUTFS, is 16× the $I_{REF}$ current.
[3]Use an external amplifier to drive any external load.
[4]Measured at $f_{CLOCK}$ = 40 MSPS and $f_{OUT}$ = 8 MHz.
[5]Measured as unbuffered voltage output into 50 Ω $R_{LOAD}$ at IOUTA, IOUTB, QOUTA, and QOUTB, $f_{CLOCK}$ = 40 MSPS and $f_{OUT}$ = 8 MHz.
Specifications subject to change without notice.

## DYNAMIC SPECIFICATIONS

**($T_{MIN}$ to $T_{MAX}$, AVDD = +5 V, DVDD = +5 V, IOUTFS = 10 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted)**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | |
| Maximum Output Update Rate | 40 | | | MSPS |
| Output Settling Time ($t_{ST}$ to 0.025%) | | 35 | | ns |
| Output Propagation Delay ($t_{PD}$) | | 55 | | Clocks[1] |
| Glitch Impulse | | 5 | | pV-s |
| Output Rise Time (10% to 90%) | | 2.5 | | ns |
| Output Fall Time (10% to 90%) | | 2.5 | | ns |
| AC LINEARITY TO NYQUIST | | | | |
| Signal-to-Noise and Distortion (SINAD) | | | | |
| $F_{OUT}$ = 5 MHz; CLOCK = 40 MHz | | TBD | | dB |
| Total Harmonic Distortion (THD) | | | | |
| $F_{OUT}$ = 5 MHz; CLOCK = 40 MHz | | TBD | | dB |
| Spurious-Free Dynamic Range (SFDR) | | | | |
| $F_{OUT}$ = 5 MHz; CLOCK = 40 MHz; 20 MHz Span | | 70 | | dB |

## DIGITAL SPECIFICATIONS

**($T_{MIN}$ to $T_{MAX}$, AVDD = +5 V, DVDD = +5 V, IOUTFS = 10 mA unless otherwise noted)**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| DIGITAL INPUTS | | | | |
| Logic "1" Voltage @ DVDD = +5 V | 3.5 | 5 | | V |
| Logic "1" Voltage @ DVDD = +3 V | 2.1 | 3 | | V |
| Logic "0" Voltage @ DVDD = +5 V | | 0 | 1.3 | V |
| Logic "0" Voltage @ DVDD = +3 V | | 0 | 0.9 | V |
| Logic "1" Current | –10 | | +10 | mA |
| Logic "0" Current | –10 | | +10 | mA |
| Input Capacitance | | 5 | | pF |
| Input Setup Time ($t_S$) | | 3 | | ns |
| Input Hold Time ($t_H$) | | 2 | | ns |
| CLOCK High | | TBD | | ns |
| CLOCK Low | | TBD | | ns |

Specifications subject to change without notice.



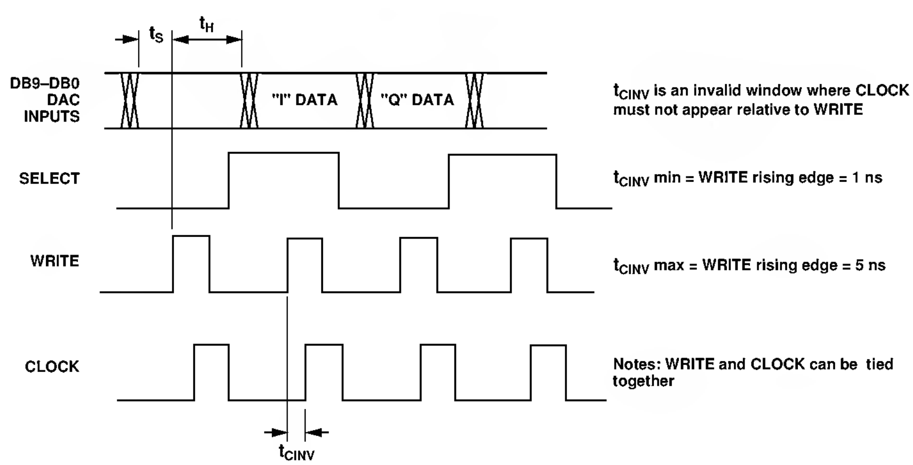



*Figure 1. Timing Diagram*

## DIGITAL FILTER SPECIFICATIONS

**($T_{MIN}$ to $T_{MAX}$, AVDD = +2.7 V to 5.5 V, DVDD = +2.7 V to 5.5 V, IOUTFS = 10 mA unless otherwise noted)**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| MAXIMUM INPUT CLOCK RATE ($F_{CLOCK}$) | 50 | | | MSPS |
| DIGITAL FILTER CHARACTERISTICS | | | | |
| Passband Width[1]: 0.005 dB | | 0.2010 | | $F_{OUT}/F_{CLOCK}$ |
| Passband Width: 0.01 dB | | 0.2025 | | $F_{OUT}/F_{CLOCK}$ |
| Passband Width: 0.1 dB | | 0.2105 | | $F_{OUT}/F_{CLOCK}$ |
| Passband Width: –3 dB | | 0.239 | | $F_{OUT}/F_{CLOCK}$ |
| Linear Phase (FIR Implementation) | | | | |
| Stopband Rejection: 0.3 $F_{CLOCK}$ to 0.7 $F_{CLOCK}$ | | –62.5 | | dB |
| Group Delay[2] | | 32 | | Input Clocks |
| Impulse Response Duration[3] | | | | |
| –40 dB | | 28 | | Input Clocks |
| –60 dB | | 40 | | Input Clocks |

NOTES
[1]Excludes SINX/X characteristic of DAC.
[2]Defined as the number of data clock cycles between impulse input and peak of output response.
[3]55 input clock periods from input to "I" DAC, 56 to "Q" DAC. Propagation delay is delay from data input to DAC update.

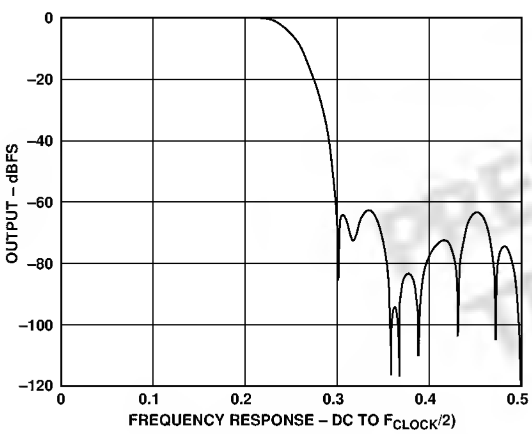



*Figure 2a. FIR Filter Frequency Response*

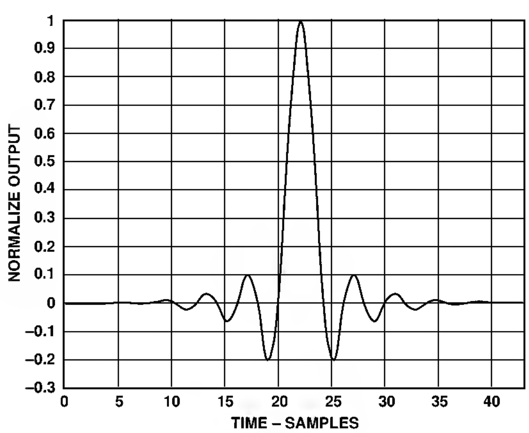



*Figure 2b. FIR Filter Impulse Response*

**Table I. Integer Filter Coefficients for 43-Tap Halfband FIR Filter**

| Lower Coefficient | Upper Coefficient | Integer Value |
|---|---|---|
| H(1) | H(43) | 1 |
| H(2) | H(42) | 0 |
| H(3) | H(41) | 3 |
| H(4) | H(40) | 0 |
| H(5) | H(39) | 8 |
| H(6) | H(38) | 0 |
| H(7) | H(37) | –16 |
| H(8) | H(36) | 0 |
| H(9) | H(35) | 29 |
| H(10) | H(34) | 0 |
| H(11) | H(33) | -50 |
| H(12) | H(32) | 0 |
| H(13) | H(31) | 81 |
| H(12) | H(30) | 0 |
| H(15) | H(29) | –131 |
| H(16) | H(28) | 0 |
| H(17) | H(27) | 216 |
| H(18) | H(26) | 0 |
| H(19) | H(25) | –400 |
| H(20) | H(24) | 0 |
| H(21) | H(23) | 1264 |
| H(24) | | 1998 |

### ORDERING GUIDE

| Model | Package Description | Package Option |
|---|---|---|
| AD9761ARS | 28-Lead Shrink Small Outline (SSOP) | RS-28 |
| AD9761-EB | Evaluation Board | |

### THERMAL CHARACTERISTICS

**Thermal Resistance**
28-Pin SSOP
$\theta_{JA}$ = 109°C/W

### ABSOLUTE MAXIMUM RATINGS*

| Parameter | With Respect to | Min | Max | Units |
|---|---|---|---|---|
| AVDD | ACOM | –0.3 | +6.5 | V |
| DVDD | DCOM | –0.3 | +6.5 | V |
| ACOM | DCOM | –0.3 | +0.3 | V |
| AVDD | DVDD | –6.5 | +6.5 | V |
| CLOCK, WRITE | DCOM | –0.3 | DVDD+0.3 | V |
| SELECT, SLEEP | DCOM | –0.3 | DVDD+0.3 | V |
| Digital Inputs | DCOM | –0.3 | DVDD+0.3 | V |
| IOUTA, IOUTB | ACOM | –1.0 | AVDD+0.3 | V |
| QOUTA, QOUTB | ACOM | –1.0 | AVDD+0.3 | V |
| COMP1, COMP2 | ACOM | –0.3 | AVDD+0.3 | V |
| COMP3 | ACOM | –0.3 | AVDD+0.3 | V |
| REFIO, FSADJ | ACOM | –0.3 | AVDD+0.3 | V |
| REFLO | ACOM | –0.3 | +0.3 | V |
| Junction Temperature | +150 | °C | | |
| Storage Temperature | –65 | +150°C | | |
| Lead Temperature (10 sec) | +300 | °C | | |

*This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

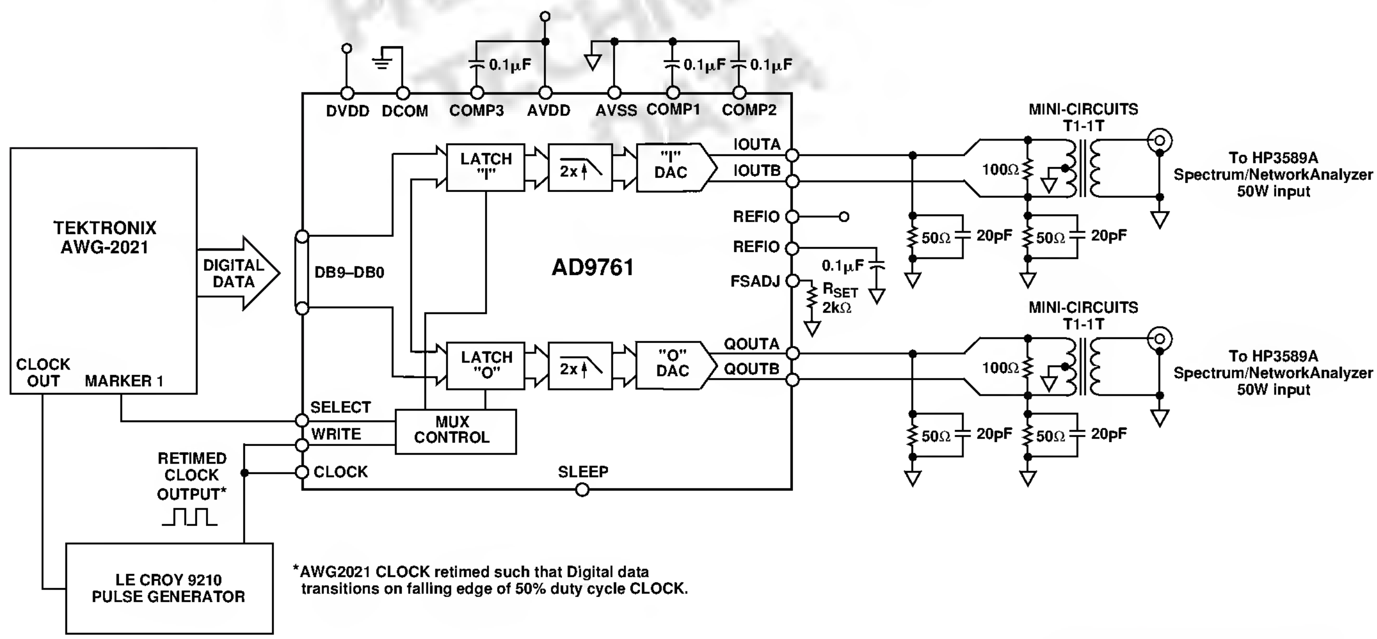



*Figure 3. Application*

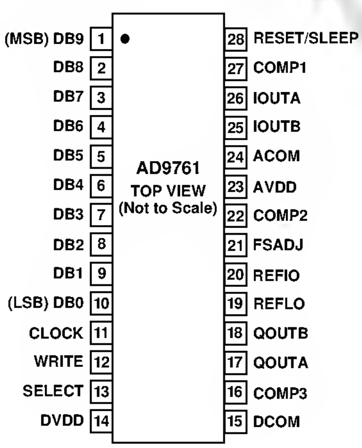
### CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9761 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN FUNCTION DESCRIPTIONS

| Pin No. | Name | Description |
|---|---|---|
| 1 | DB9 | Most Significant Data Bit (MSB). |
| 2–9 | DB8–DB1 | Data Bits 1-8. |
| 10 | DB0 | Least Significant Data Bit (LSB). |
| 11 | CLOCK | Clock Input. Both DACs' outputs updated on positive edge of clock and digital filters read respective input registers. |
| 12 | WRITE | Write input. DAC input registers latched on positive edge of write. |
| 13 | SELECT | Select Input. Select high routes input data to "I" DAC, select low routes data to "Q" DAC. |
| 14 | DVDD | Digital Supply Voltage (+2.7 V to +5.5 V). |
| 15 | DGND | Digital Ground. |
| 16 | COMP3 | Internal Bias Node for Switch Driver Circuitry. Decouple to AGND with 0.1 μF capacitor. |
| 17 | QOUTA | "Q" DAC Current Output. Full-scale current when all data bits are 1s. |
| 18 | QOUTB | "Q" DAC Complementary Current Output. Full-scale current when all data bits are 0s. |
| 19 | REFLO | Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference. |
| 20 | REFIO | Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.2 reference output when internal reference activated. Requires 0.1 μF capacitor to ACOM when internal reference activated. |
| 21 | FSADJ | Full-Scale Current Output Adjust. |
| 22 | COMP2 | Bandwidth/Noise Reduction Node. Add 0.1 μF to AVDD for optimum performance. |
| 23 | AVDD | Analog Supply Voltage (+2.7 V to +5.5 V). |
| 24 | AGND | Analog Common. |
| 25 | IOUTB | As 18 only "I" DAC. |
| 26 | IOUTA | As 17 only "I" DAC. |
| 27 | COMP1 | As COMP3 (Pin 16). |
| 28 | RESET/SLEEP | Power-Down Control Input If Asserted for Four Clock Cycles or Longer. Reset control input if asserted for less than four clock cycles. Active high. Connect to DGND if not used. Refer to RESET/SLEEP section. |

## PIN CONFIGURATION



## DEFINITIONS OF SPECIFICATIONS

**Linearity Error (Also Called Integral Nonlinearity or INL)**
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

**Differential Nonlinearity (or DNL)**
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

**Monotonicity**
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

**Offset Error**
The deviation of the output current from the ideal of zero is called offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

**Gain Error**
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

**Output Compliance Range**
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

**Temperature Drift**
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either $T_{MIN}$ or $T_{MAX}$. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

**Power Supply Rejection**
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

**Settling Time**
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

**Glitch Impulse**
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified the net area of the glitch in pV-s.

**Spurious-Free Dynamic Range**
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

**Total Harmonic Distortion**
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

**Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio**
S/N+D is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

**Passband**
Frequency band in which any input applied therein passes unattenuated to the DAC output.

**Stopband Rejection**
The amount of attenuation of a frequency outside the passband applied to the DAC, relative to a full-scale signal applied at the DAC input within the passband.

**Group Delay**
Number of input clocks between an impulse applied at the device input and peak DAC output current.

**Impulse Response**
Response of the device to an impulse applied to the input.

# AD9761–Typical AC Characterization Curves @ +5 V Supplies

**(AVDD = +5 V, DVDD = +5 V, 50 Ω Doubly Terminated Load, Differential Output, $T_A$ = +25°C, SFDR up to Nyquist, unless otherwise noted)**

*Figure 4. TBD*

*Figure 5. TBD*

*Figure 6. TBD*

*Figure 7. TBD*

*Figure 8. TBD*

*Figure 9. TBD*

*Figure 10. TBD*

*Figure 11. TBD*

*Figure 12. TBD*

# AD9761-Other Characterization Curves @ +5V Supplies

**(AVDD = +5 V, DVDD = +5 V, 50 Ω Doubly Terminated Load, Differential Output, $T_A$ = +25°C, SFDR up to Nyquist, unless otherwise noted)**

*Figure 13. TBD*

*Figure 14. TBD*

*Figure 15. TBD*

*Figure 16. TBD*

*Figure 17. TBD*

*Figure 18. TBD*

*Figure 19. TBD*

*Figure 20. TBD*

*Figure 21. TBD*

## FUNCTIONAL DESCRIPTION

Figure 22 shows a simplified block diagram of the AD9761. The AD9761 is a complete dual channel, high speed, 10 bit CMOS DAC capable of operating up to a 40 MHz clock rate. It has been optimized for the transmit section of wideband communication systems employing I and Q modulation schemes. Excellent matching characteristics between channels reduces the need for any external calibration circuitry. Dual matching 2× interpolation filters included in the "I" and "Q" data path simplify any post, bandlimiting filter requirements. The AD9761 interfaces with a single 10-bit digital input bus that supports interleaved "I" and "Q" input data.

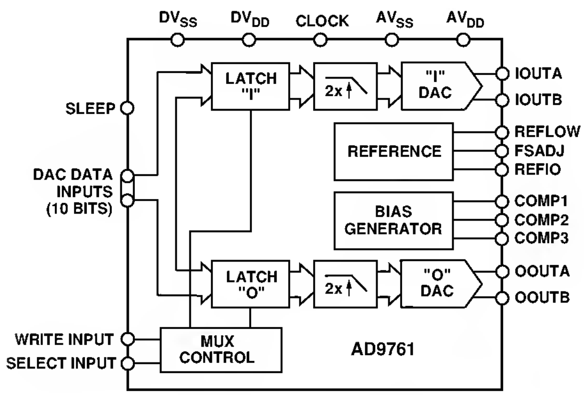



*Figure 22. Dual DAC Functional Block Diagram*

Referring to Figure 22, the AD9761 consists of an analog section and a digital section. The analog section includes matched "I" and "Q" 10-bit DACs, a 1.20 V bandgap voltage reference and a reference control amplifier. The digital section includes: two 2× interpolation filters; segment decoding logic; and some additional digital input interface circuitry. The analog and digital sections of the AD9761 have separate power supply inputs (i.e., AVDD and DVDD) which can operate over a 2.7 V to 5.5 V range.

Each DAC consists of a large PMOS current source array capable of providing up to 10 mA of full-scale current, $I_{OUTFS}$. Each array is divided into 15 equal currents which make up the four most significant bits (MSBs). The next four bits or middle bits consist of 15 equal current sources whose value are 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle-bits current sources. All of these current sources are switched to one or the other of two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches.

The full-scale output current, $I_{OUTFS}$, of each DAC is regulated from the same voltage reference and control amplifier thus ensuring excellent gain matching and drift characteristics between DACs. $I_{OUTFS}$ can be set from 1 mA to 10 mA via an external resistor, $R_{SET}$. The external resistor in combination with both the reference control amplifier and voltage reference, $V_{REFIO}$, sets the reference current, $I_{REF}$, which is mirrored over to the segmented current sources with the proper scaling factor. $I_{OUTFS}$ is exactly sixteen times the value of $I_{REF}$.

The "I" and "Q" DACs are updated simultaneously on the rising edge of CLOCK with digital data from their respective 2× digital interpolation filters. The 2× interpolation filters essentially multiply the input data rate of each DAC by a factor of two relative to its original input data rate while simultaneously reducing the magnitude of first image associated with the DAC's original input data rate. Since the AD9761 supports a single 10-bit digital bus with interleaved "I" and "Q" input data, the original "I" and "Q input data rate before interpolation is one-half the CLOCK rate. After interpolation, the data rate into each "I" and "Q" DAC becomes equal to the CLOCK rate.

The benefits of an interpolation filter are clearly seen in Figure 23 which shows an example of the frequency and time domain representation of a discrete time sine wave signal before and after it is applied to a digital interpolation filter. Images of the sine wave signal appear around multiples of the DAC's input data rate as predicted by the sampling theory. These undesirable images will also appear at the output of a reconstruction DAC, although modified by the DAC's sin(x)/(x) response. In many bandlimited applications, these images must be suppressed by an analog filter following the DAC. The complexity of this analog filter is typically determined by the proximity of the desired fundamental to the first image and the required amount of image suppression.

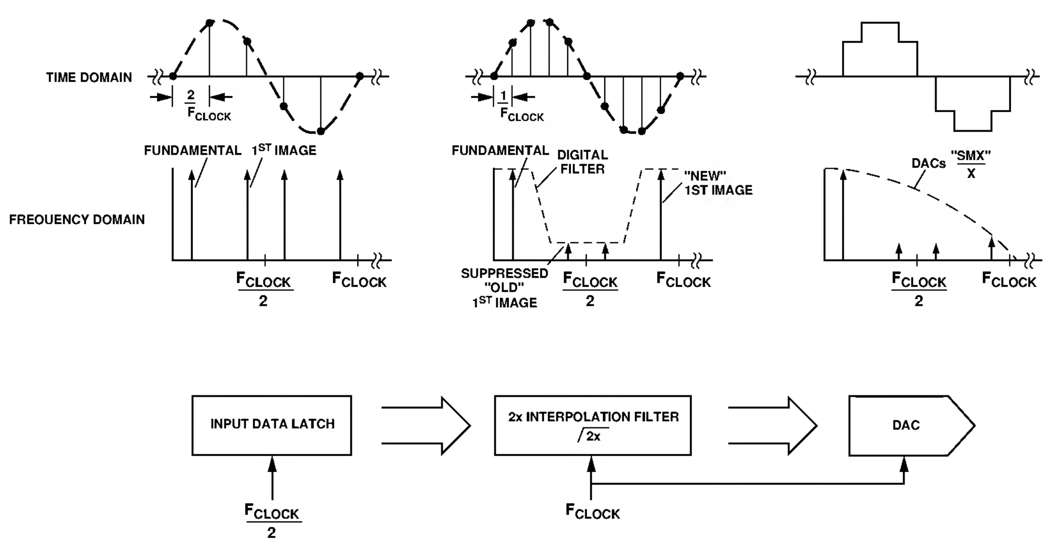



*Figure 23. Time and Frequency Domain Example of Digital Interpolation Filter*

Referring to Figure 23, the "new" first image associated with the DAC's higher data rate *after* interpolation is "pushed" out further relative to the input signal. The "old" first image associated with the lower DAC data rate *before* interpolation is suppressed by the digital filter. As a result, the transition band for the analog reconstruction filter is increased thus reducing the complexity of the analog filter.

The digital interpolation filters for "I" and "Q" paths are identical 43 tap halfband symmetric FIR filters. Each filter receives de-interleaved "I" or "Q" data from the digital input interface. The input CLOCK signal is internally divided by two to generate the filter clock. The filters are implemented with two parallel paths running at the filter clock rate. The output from each path is selected on opposite phases of the filter clock thus producing interpolated filtered output data at the input clock rate. The frequency response and impulse response of these filters are shown in Figure 2a and 2b. Table I lists the idealized filter coefficients which correspond to the filter's impulse response.

The digital section of the AD9761 also includes an input interface section designed to support interleaved "I" and "Q" input data off a single 10-bit bus. This section de-interleaves the "I" and "Q" input data while ensuring its proper pairing for the 2× interpolation filters. A SLEEP input serves a dual function by providing a reset function for this section as well as providing power down functionality. Refer to the DIGITAL INPUT AND INTERFACE CONSIDERATIONS and SLEEP sections for a more detailed discussion.

## DAC TRANSFER FUNCTION

Each "I" and "Q" DAC provide complementary current output pins: IOUT(A/B) and QOUT(A/B) respectively. Note, QOUTA and QOUTB operate identical to IOUTA and IOUTB. IOUTA will provide a near full-scale current output, $I_{OUTFS}$, when all bits are high (i.e., DAC CODE = 1023) while IOUTB, the complementary output, provides no current. The current output of IOUTA and IOUTB are a function of both the input code and $I_{OUTFS}$ and can be expressed as:

$$I_{IOUTA} = (DAC\ CODE/1024) \times I_{OUTFS} \tag{1}$$

$$I_{IOUTB} = (1023 - DAC\ CODE)/1024 \times I_{OUTFS} \tag{2}$$

where:

DAC CODE = 0 to 1023 (i.e., Decimal Representation).

As mentioned previously, $I_{OUTFS}$ is a function of the reference current, $I_{REF}$, which is nominally set by a reference, $V_{REFIO}$, and external resistor, $R_{SET}$. It can be expressed as:

$$I_{OUTFS} = 16 \times I_{REF} \tag{3}$$

where:

$$IREF = VREFIO/R_{SET} \tag{4}$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, $R_{LOAD}$, which are tied to analog common, ACOM. Note, $R_{LOAD}$ represents the equivalent load resistance seen by IOUTA or IOUTB. The single-ended voltage output appearing at IOUTA and IOUTB pins is simply:

$$VIOUTA = IIOUTA \times R_{LOAD} \tag{5}$$

$$VIOUTB = IIOUTB \times R_{LOAD} \tag{6}$$

Note, the full-scale value of $V_{IOUTA}$ and $V_{IOUTB}$ should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

The differential voltage, $V_{IDIFF}$, appearing across IOUTA and IOUTB is:

$$V_{IDIFF} = (I_{IOUTA} - I_{IOUTB}) \times R_{LOAD} \tag{7}$$

Substituting the values of $I_{IOUTA}$, $I_{IOUTB}$, and $I_{REF}$; $V_{IDIFF}$ can be expressed as:

$$V_{IDIFF} = \{(2\ DAC\ CODE - 1023)/1024)\} \times (16\ R_{LOAD}/R_{SET}) \times V_{REFIO} \tag{8}$$

These last two equations highlight some of the advantages of operating the AD9761 differentially. First, differential operation will help cancel common-mode error sources associated with $I_{IOUTA}$ and $I_{IOUTB}$ such as noise and distortion. Second, the differential code dependent current and subsequent voltage, $V_{IDIFF}$, is twice the value of the single-ended voltage output (i.e., $V_{IOUTA}$ or $V_{IOUTB}$) thus providing twice the signal power to the load.

## REFERENCE OPERATION

The AD9761 contains an internal 1.20 V bandgap reference which can be easily disabled and overridden by an external reference. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is selected. If REFLO is tied to ACOM as shown in Figure 24, the internal reference is activated and REFIO provides a 1.20 V output. In this case, the internal reference must be compensated externally with a ceramic chip capacitor of 0.1 µF or greater from REFIO to REFLO. Also, REFIO should be buffered with an external amplifier having a low input bias current (i.e., <1 µA) if any additional loading is required.

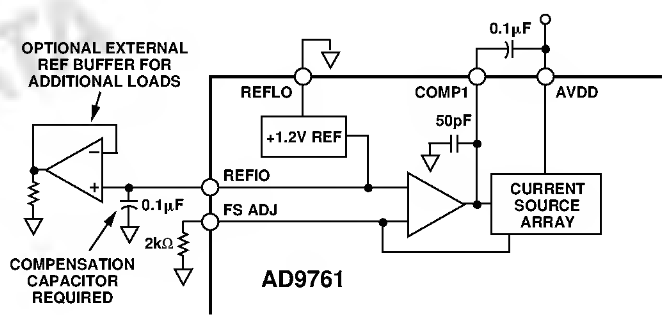



*Figure 24. Internal Reference Configuration*

The internal reference can also be disabled by connecting REFLO to AVDD. In this case, an external reference may then be applied to REFIO as shown in Figure 25. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is disabled and the high input impedance (i.e., 1 MΩ) of REFIO minimizes any loading of the external reference.

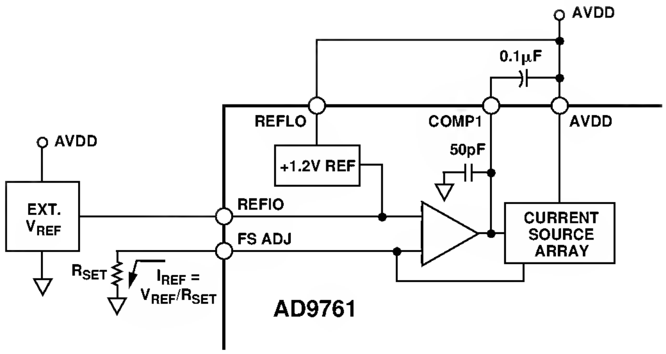



*Figure 25. External Reference Configuration*

Depending on the requirements of the application, $I_{REF}$ can be adjusted by varying either $R_{SET}$, or in the external reference mode, by varying the REFIO voltage. $I_{REF}$ can be varied for a fixed $R_{SET}$ by disabling the internal reference and varying the voltage of REFIO over its compliance range of 1.25 V to 0.10 V. REFIO can be driven by a single-supply amplifier or DAC thus allowing $I_{REF}$ to be varied for a fixed $R_{SET}$. Since the input impedance of REFIO is approximately 1 MΩ, a simple, low cost R-2R ladder DAC configured in the voltage mode topology may be used to control the gain. This circuit is shown in Figure 26 using the AD7524 and an external 1.2 V reference, the AD1580.

## REFERENCE CONTROL AMPLIFIER

The AD9761 also contains an internal control amplifier which is used to simultaneously regulate both DAC's full-scale output current, $I_{OUTFS}$. Since the "I" and "Q" $I_{OUTFS}$ are derived from the same voltage reference and control circuitry, excellent gain matching is ensured. The control amplifier is configured as a V-I converter as shown in Figure 25 such that its current output, $I_{REF}$, is determined by the ratio of the $V_{REFIO}$ and an external resistor, $R_{SET}$, as stated in Equation (4). $I_{REF}$ is copied over to the segmented current sources with the proper scaling factor to set $I_{OUTFS}$ as stated in Equation (3).

The control amplifier allows a wide (10:1) adjustment span of $I_{OUTFS}$ over a 1 mA to 10 mA range by setting $I_{REF}$ between 62.5 µA and 625 µA. The wide adjustment span of $I_{OUTFS}$ provides several application benefits. The first benefit relates directly to the power dissipation of the AD9761's analog supply, AVDD, which is proportional to $I_{OUTFS}$ (refer to the POWER DISSIPATION section). The second benefit relates to the 20 dB adjustment span which may be useful for system gain control purposes.

Optimum noise and dynamic performance for the AD9761 is obtained with a 0.1 µF external capacitor installed between COMP2 and AVDD. The bandwidth of the reference control amplifier is limited to approximately 5 kHz with a 0.1 µF capacitor installed. Since the –3 dB bandwidth corresponds to the dominant pole and hence its dominant time constant, the settling time of the control amplifier to a stepped reference input response can be easily determined. Note, the output of the control amplifier, COMP2, is internally compensated via a 50 pF capacitor thus ensuring its stability if no external capacitor is added.

## ANALOG OUTPUTS

As previously stated, both the "I" and "Q" DACs produce two complementary current outputs which may be configured for single-end or differential operation. $I_{IOUTA}$ and $I_{IOUTB}$ can be converted into complementary single-ended voltage outputs, $V_{IOUTA}$ and $V_{IOUTB}$, via a load resistor, $R_{LOAD}$, as described in the DAC TRANSFER SECTION by Equations 5 through 8. The differential voltage, $V_{IDIFF}$, existing between $V_{IOUTA}$ and $V_{IOUTB}$ can also be converted to a single-ended voltage via a transformer or differential amplifier configuration.

Figure 27 shows an equivalent circuit of the AD9761's "I" (or "Q") DAC output. It consists of a parallel array of PMOS current sources in which each current source is switched to either IOUTA or IOUTB via a differential PMOS switch. As a result, the equivalent output impedance of IOUTA and IOUTB remains quite high (i.e., >100 kΩ and 5 pF).

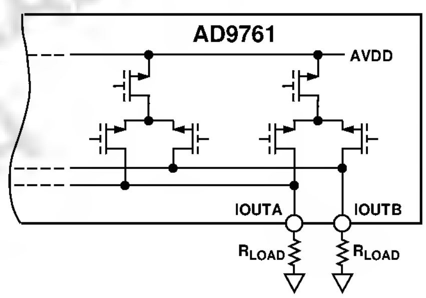



*Figure 27. Equivalent Circuit of the AD9761 DAC Output*

IOUTA and IOUTB have a negative and positive voltage compliance range which must be adhered to achieve optimum performance. The negative output compliance range of –1 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage.

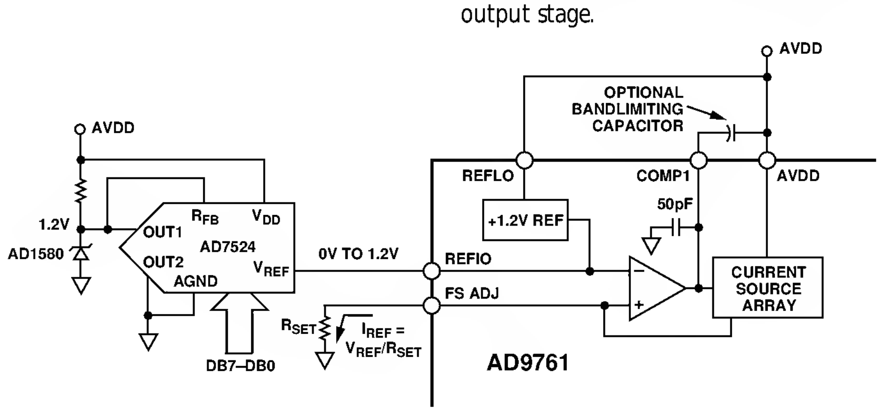



*Figure 26. Single-Supply Gain Control Circuit*

The positive output compliance range is slightly dependent on the full-scale output current, $I_{OUTFS}$. It degrades slightly from its nominal 1.25 V for an IOUTFS = 10 mA to 1.00 V for an IOUTFS = 2 mA. Applications requiring the AD9761's output (i.e., $V_{OUTA}$ and/or $V_{OUTB}$) to extend to its output compliance range should size $R_{LOAD}$ accordingly. Operation beyond this compliance range will adversely affect the AD9761's linearity performance and subsequently degrade its distortion performance. Note, the optimum distortion performance of the AD9761 is obtained by restricting its output(s) as seen at IOUT(A/B) and QOUT(A/B) to within ±0.5 V.

## DIGITAL INPUTS AND INTERLEAVED INTERFACE CONSIDERATIONS

The AD9761 digital interface consists of 10 data input pins, a clock input pin, and three control pins. It is designed to support a clock rate up to 40 MSPS. The 10-bit parallel data inputs follow standard positive binary coding, where DB9 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). IOUTA (or QOUTA) produces a full-scale output current when all data bits are at logic 1. IOUTB (or QOUTB) produces a complementary output, with the full-scale current split between the two outputs as a function of the input code.

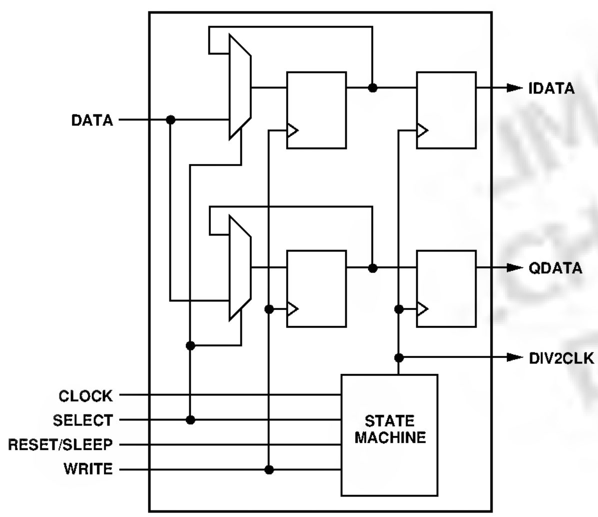



*Figure 28. Block Diagram of Digital Interface*

The AD9761 interfaces with a single 10-bit digital input bus that supports interleaved "I" and "Q" input data. Figure 28 shows a simplified block diagram of the digital interface circuitry consisting of edge triggered registers, two multiplexes, and a state machine. Interleaved "I" and "Q" input data is presented at the DATA input bus, where it is then latched into the selected "I" or "Q" data register on the rising edge of the WRITE input. The output of these data registers is transferred in pairs to the interpolator filters' inputs after each "Q" write on the rising edge of the CLOCK input (refer to Timing Diagram in Figure 2). A state machine ensures the proper pairing of "I" and "Q" input data to the interpolation filter's inputs.

The SELECT signal at the time of the rising edge of the WRITE signal determines which data register latches the input data. If SELECT is high around the rising edge of WRITE the data is latched into the "I" register of the AD9761. If SELECT is low around the rising edge of the WRITE, the data is latched into the "Q" register of the AD9761. If SELECT is kept in one state while data is repeatedly writing to the AD9761, the data will be written into the selected register at half the input data rate since the data is always assumed to be interleaved.

The state machine controls the generation of the divided clock and hence pairing of "I" and "Q" data inputs. After the AD9761 is reset, the state machine keeps track of the paired "I" and "Q" data. The state transition diagram is shown in Figure 29 in which all the states are defined. A transition in state occurs upon the rising edge of CLOCK and is function of the current state as well as status of SELECT, WRITE, and SLEEP. The state machine can be reset by asserting a logic level "1" to the SLEEP input for less than four clock cycles. The most recent "I" and "Q" data samples are transferred to the correct interpolation filter only upon entering state PAIR.

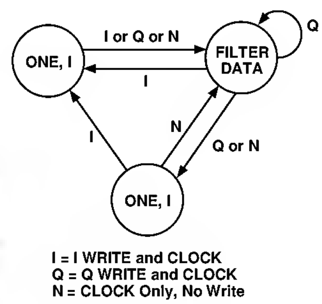



*Figure 29. State Transition Diagram of AD9761 Digital Interface*

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$ set to approximately half the digital positive supply (DVDD) or $V_{THRESHOLD}$ = DVDD/2 (±20%).

The internal digital circuitry of the AD9761 is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage, $V_{OH(MAX)}$, of the TTL drivers. A DVDD of 3 V to 3.3 V will typically ensure proper compatibility of most TTL logic families. Figure 30 shows the equivalent digital input circuit for the data, sleep, and clock inputs.

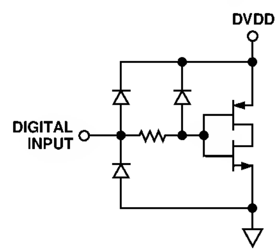



*Figure 30. Equivalent Digital Input*

Since the AD9761 is capable of being updated up to 40 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum set-up and hold-times of the AD9761 as well as its required min/max input logic level thresholds. The external clock driver circuitry should provide the AD9761 with a low jitter clock input meeting the min/max logic levels while providing

fast edges. Fast clock edges will help minimize any jitter which can manifest itself as phase noise on a reconstructed waveform.

Digital signal paths should be kept short, and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9761 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs which contributes to data feedthrough. Also, operating the AD9761 with reduced logic swings and a corresponding digital supply (DVDD) will also reduce data feedthrough.

## RESET/SLEEP MODE OPERATION

The RESET/SLEEP input can be used to either power-down the AD9761 or reset its internal digital interface logic. If the RESET/SLEEP input is asserted for under four clock cycles by applying a logic level "1," the internal state machine will be reset. However, if the RESET/SLEEP input is asserted for four clock cycles or longer, the power-down function of the AD9761 will be initiated. The power-down function turns off the output current and reduces the supply current to less than 9 mA over the specified supply range of 2.7 V to 5.5 V and temperature range.

The power-up and power-down characteristics of the AD9761 is dependent upon the value of the compensation capacitor connected to COMP1 and COMP3. With a nominal value of 0.1 µF, the AD9761 takes less than 5 µs to power down and approximately 3.25 ms to power back up.

## POWER DISSIPATION

The power dissipation, $P_D$, of the AD9761 is dependent on several factors which include: (1) AVDD and DVDD, the power supply voltages; (2) $I_{OUTFS}$, the full-scale current output; (3) $F_{CLOCK}$, the update rate; (4) and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, $I_{AVDD}$, and the digital supply current, $I_{DVDD}$. $I_{AVDD}$ is directly proportional to $I_{OUTFS}$ as shown in Figure 46 and is insensitive to $F_{CLOCK}$.

**TBD**

*Figure 31. $I_{AVDD}$ vs. $I_{OUTFS}$*

Conversely, $I_{DVDD}$ is dependent on both the digital input waveform, $F_{CLOCK}$, and digital supply DVDD. Figures 32 and 33 show $I_{DVDD}$ as a function of a full-scale sine wave output ratio's ($F_{OUT}/F_{CLOCK}$) for various update rate with DVDD = 5 V and DVDD = 3 V respectively. Note, how $I_{DVDD}$ is reduced by more than a factor of 2 when DVDD is reduced from 5.0 V to 3 V.

**TBD**

*Figure 32. $I_{DVDD}$ vs. Ratio @ DVDD = 5 V*

**TBD**

*Figure 33. $I_{DVDD}$ vs. Ratio @ DVDD = 3 V*

## APPLYING THE AD9761

### OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9761. Unless otherwise noted, it is assumed that $I_{OUTFS}$ is set to a nominal 10 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an appropriately sized load resistor, $R_{LOAD}$, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter thus converting $I_{OUTA}$ or $I_{OUTB}$ into a negative unipolar voltage. This configuration provides the best dc linearity since IOUTA or IOUTB is maintained at a virtual ground.

### DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 49. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformers passband. An RF transformer such as the Mini Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

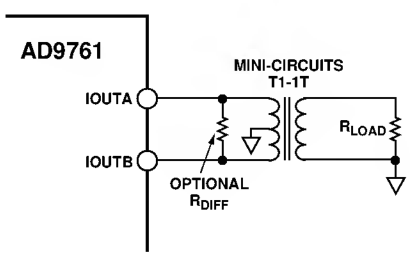



*Figure 34. Differential Output Using a Transformer*

The center-tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both $I_{OUTA}$ and $I_{OUTB}$. The complementary voltages appearing at IOUTA and IOUTB (i.e., $V_{OUTA}$ and $V_{OUTB}$) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9761. A differential resistor, $R_{DIFF}$, may be inserted in applications in which the output of the transformer is connected to the load, $R_{LOAD}$, via a passive reconstruction filter or cable requiring double termination. $R_{DIFF}$ is determined by the transformer's impedance ratio and provides the proper source termination which results in a low VSWR. Note that approximately half the signal power will be dissipated across $R_{DIFF}$.

### DIFFERENTIAL USING AN OP AMP

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 35. The AD9761 is configured with two equal load resistors, $R_{LOAD}$, of 50 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amps distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

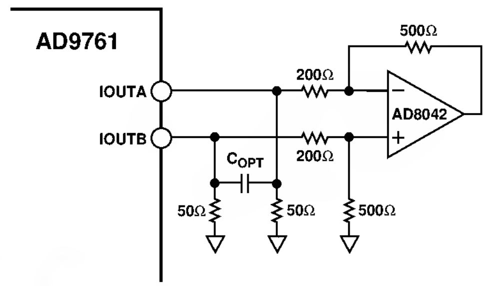



*Figure 35. DC Differential Coupling Using an Op Amp*

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8042 is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9761 while meeting other system level objectives (i.e., cost, power) should be selected. The op amps differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 36 provides the necessary level-shifting required in a single supply system. In this case, AVDD which is the positive analog supply for both the AD9761 and the op amp is also used to level-shift the differential output of the AD9761 to midsupply (i.e., AVDD/2).

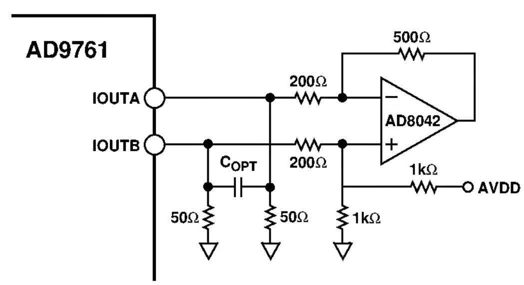



*Figure 36. Single-Supply DC Differential Coupled Circuit*

### SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 37 shows the AD9761 configured to provide a unipolar output range of approximately 0 V to +1.0 V since the nominal full-scale current, $I_{OUTFS}$, of 10 mA flows through an $R_{LOAD}$ of 100 Ω. In the case of a doubly terminated low-pass filter, $R_{LOAD}$ represents the equivalent load resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching $R_{LOAD}$. Different

values of $I_{OUTFS}$ and $R_{LOAD}$ can be selected as long as the positive compliance range is adhered to.

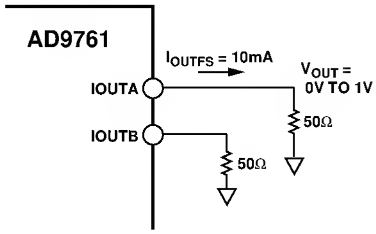



*Figure 37. 0 V to +0.5 V Unbuffered Voltage Output*

**DIFFERENTIAL, DC COUPLED OUTPUT CONFIGURATION WITH LEVEL SHIFTING**

Some applications may require the AD9761 differential outputs to interface to a single supply quadrature upconverter. Although most of these devices provide differential inputs, its common-mode voltage range does not typically extend to ground. As a result, the ground-referenced output signals shown in Figure 37 must be level shifted to within the specified common-mode range of the single-supply quadrature upconverter. Figure 38 shows the addition of a resistor pull-up network which provides the level shifting function. The use of matched resistor networks will maintain maximum gain matching and minimum offset performance between the I and Q channels. Note, the resistor pull-up network will introduce approximately 6 dB of signal attenuation.

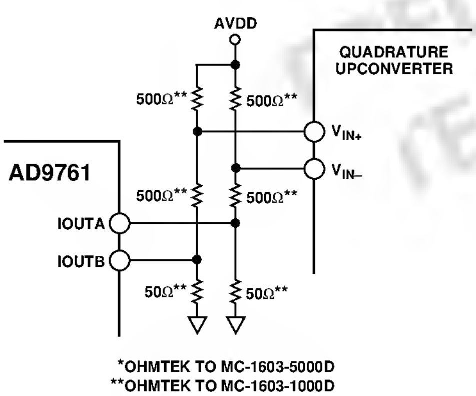



*Figure 38. Differential, DC Coupled Output Configuration with Level-Shifting.*

**POWER AND GROUNDING CONSIDERATIONS**

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection; placement and routing; and supply bypassing and grounding. The evaluation board for the AD9761 which uses a four layer PC board serves as a good example for the above mentioned considerations. The evaluation board provides an illustration of the recommended printed circuit board ground, power, and signal plane layout.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9761 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply should be decoupled to DCOM as close as physically as possible.

For those applications that require a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 39. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

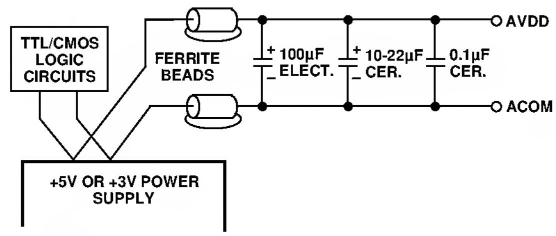



*Figure 39. Differential LC Filter for Single +5 V or +3 V Applications*

Maintaining low noise on power supplies and ground is critical to obtaining optimum results from the AD9762. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces and the digital ground plane confined to areas covering the digital interconnects.

All analog ground pins of the DAC, reference, and other analog components, should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal, and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part, as well as, providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. Its is recommended that all connections be short, direct and as physically close to the package as possible, in order to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistor should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' application notes AN-280 and AN-333.

## APPLICATIONS

### Using the AD9761 for QAM Modulation

QAM is one of the most widely used digital modulation schemes in digital communication systems. This modulation technique can be found in both FDM as well as spread spectrum (i.e., CDMA) based systems. A QAM signal is a carrier frequency which is both modulated in amplitude (i.e., AM modulation) and in phase (i.e., PM modulation). It can be generated by independently modulating two carriers of identical frequency but with a 90° phase difference. This results in an in-phase (I) carrier component and a quadrature (Q) carrier component at a 90° phase shift with respect to the I component. The I and Q components are then summed to provide a QAM signal at the specified carrier frequency.

A common and traditional implementation of a QAM modulator is shown in Figure 40. The modulation is performed in the analog domain in which two DACs are used to generate the baseband I and Q components, respectively. Each component is then typically filtered applied to a Nyquist filter before being applied to a quadrature mixer. The matching Nyquist filters shapes and limits each components spectral envelope while minimizing intersymbol interference. The DAC is typically updated at the QAM symbol rate or possibly a multiple of it if an interpolating filter precedes the DAC. The use of an interpolating filter typically eases the implementation and complexity of the analog filter which can be a significant contributor to mismatches in gain and phase between the two baseboard channels. A quadrature mixer modulates the I and Q components with in-phase and quadrature phase carrier frequency and then sums the two outputs to provide the QAM signal.

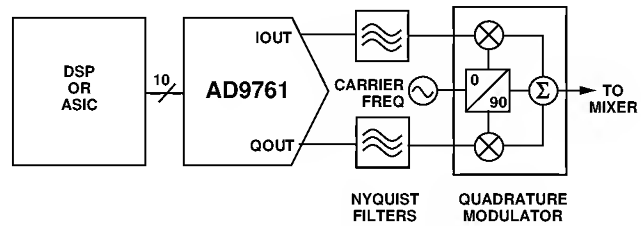



*Figure 40. Typical Analog QAM Architecture*

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 28-Lead Shrink Small Outline Package (SSOP) (RS-28)